REMARKS

In the Office Action of February 1, 2007, the Examiner (1) rejected claim 9 under 35 U.S.C. § 103(a) as allegedly obvious over U.S. Patent No. 6,041,399 ("Terada") in view of U.S. Patent No. 5,659,722 ("Blaner"); (2) rejected claims 11-13, 16, and 18 as allegedly obvious over Terada in view of U.S. Patent No. 6,088,786 ("Feierbach et al."); (3); rejected claim 10 as allegedly obvious over Terada in view of Blaner and U.S. Patent No. 5,504,903 ("Chen et al."); (4); rejected claims 14-15 and 17 as allegedly obvious over Terada in view of Blaner and Feierbach; (5) rejected claims 1-3, and 6 as allegedly obvious over Terada in view of U.S. Patent No. 6,931,632 ("Ramasamy et al."); (6) rejected claims 4-5 and 7-8 as allegedly obvious over Terada in view of Ramasamy and Blaner; (7) rejected claims 19-20 as allegedly obvious over Terada in view of Ramasamy and U.S. Patent No. 5,638,525 ("Hammond et al.").

In this Response, Applicants amend claims 1, 3, 5, 8, 11, 13, 15, and 19, cancel claims 2, 4, 6, 7, 12, 14, 16, and 17, and submit new claims 21 and 22. Based on the amendments and arguments presented herein, Applicants respectfully request reconsideration and allowance of the pending claims.

Claim 1 has been amended to require that the:

> test and skip instruction includes at least one bit that specifies whether the register reference is to a register from a first group of registers or to a register from a second group of registers, and if a register from the first group of registers is specified by said at least one bit, the comparison is performed by comparing the immediate value to the register value, and, if a register from the second group of registers is specified by said at least one bit, the comparison is performed by masking the register value with the immediate value and examining one or more bits in the masked version of the referenced register

Thus, claim 1 requires the test and skip instruction to be capable of at least two different types of comparisons—one comparison in which the immediate value is directly compared to the contents of the register and another comparison in which immediate value masks the contents of the register. Applicants believe that the Examiner has stated that Terada teaches the direct comparison of an immediate value to a register and that

Blaner teaches the masking type of comparison. Without conceding whether the Examiner's analysis is correc, none of the art of record teaches an instruction that has at least one bit that specifies which of at least two different types of comparison actions are to be performed. Combining Blaner with Terada would result in the replacement of Terada's comparison of the immediate value to a register value with a masking type of comparison. The combination of Terada and Blaner would not result in an instruction that can selectively perform either type of comparison based on a bit in the instruction. None of the other art of record satisfies the deficiencies of Terada and Blaner. For at least this reason, claim 1 and its dependent claims are allowable over the art of record. Various of the claims that depend from claim 1 have been canceled or amended based on the amendments made to claim 1.

Claim 9 requires that, if an instruction's control bit "is in a first state, comparing the immediate value to the contents of the register referenced in the instruction and skipping a subsequent instruction based on the outcome of the comparison; or if said control bit is in a second state, masking the contents of the register with the immediate value, testing one or more bits in the masked version of the contents of the register, and skipping a subsequent instruction based on the outcome of the testing." Claim 9 and dependent claim 10 are allowable over the art of record for much the same reasons as articulated above.

Claim 11 requires that:

> the instruction includes at least one bit that specifies whether the register reference is to a register from a first group of registers or to a register from a second group of registers, and if a register from the first group of registers is specified by said at least one bit, the comparison is performed by comparing the immediate value to the register value, and, if a register from the second group of registers is specified by said at least one bit, the comparison is performed by masking the register value with the immediate value and examining one or more bits in the masked version of the referenced register

Claim 11 and its dependent claims are allowable over the art of record for much the same reasons as articulated above. Various of the claims that depend from claim 11 have been canceled or amended based on the amendments made to claim 11.

Claim 19 requires that:

> said control bit selectively specifies whether the comparison is to be performed by comparing the immediate value to the register value or whether the comparison is to be performed by masking the register value with the immediate value and examining one or more bits in the masked version of the referenced register

Claim 19 and dependent claim 20 are allowable over the art of record for much the same reasons as articulated above.

Claims 21 and 22 have been added as dependent claims depending on claims 1 and 11, respectively. Because claims 21 and 22 inherit the limitations of claims 1 and 11, which are allowable as explained above, claims 21 and 22 are allowable for at least the same reason.

CONCLUSION

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants believe a two-month time extension may be necessary for this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

/Jonathan M. Harris/
Jonathan M. Harris
PTO Reg. No. 44,144
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
AGENT FOR APPLICANTS